DC reference sources

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Overview

• Voltage sources
  (Main part) ➔ Basics and Implementations

• Current sources ➔ Basics and Implementations
**Ideal voltage source**

- Output voltage *independent* of $I$, $T$, ........

**Ideal current source**

- Output current *independent* of $V$, $T$, ........

**Practical voltage source**

- Beyond $I_{th}$ a voltage source
- Output voltage *depends on* external parameters

**Practical current source**

- Beyond $V_{th}$ a current source
- Output current *depends on* external parameters
Quality Aspects V,I Source

- Output impedance
- Noise level
- Temperature dependency

Power Supply Rejection Ratio

- V,I source powered by a power source

PSRR is a measure for the sensitivity of the output quantity (V,I) for power supply variations

\[
PSRR = 20 \cdot 10^{ \left( \frac{dV_{\text{ref}}}{dV_{\text{supply}}} \cdot \frac{V_{\text{ref}}}{V_{\text{supply}}} \right) } \quad \text{unit: dB}
\]

\[
PSRR = 20 \cdot 10^{ \left( \frac{dI_{\text{ref}}}{dI_{\text{supply}}} \cdot \frac{I_{\text{ref}}}{I_{\text{supply}}} \right) } \quad \text{unit: dB}
\]

- The larger the better
**Voltage sources**

Simple  \(\rightarrow\) Quality  \(\rightarrow\) Complicated

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**Most simple voltage source**

- Accuracy depends on \(V_{cc}\) and matching of \(R_1\) and \(R_2\)
- Low output impedance and low noise costs *power* or a *capacitor*
- \(\text{PSRR} = 1\)
  
  Can also be improved by *capacitor*

\[
V_{\text{ref}} = V_{cc} \frac{R_2}{R_1 + R_2}
\]
Non-linear voltage divider

A. Diode-connected transistor
B. Zener diode \( \rightarrow \) Zener and Avalanche breakdown
C. Normally-off FET (NMOS)
D. Bipolar transistor at punch-through

Reference Sources
A. van Staveren and W.A. Serdijn

Zener breakdown

Electron must gain energy equal to \( E_g \) for a transition from valence band to conduction band

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Avalanche breakdown

- Electrons are accelerated by E-field
- Speed high enough ➔ other electrons are made free

Requirements:
- **E-field** must be high enough
- **Free path length** must be high enough

Positive t.c.
Dominant $V_r > 6$V
**Temperature compensation Zener diode**

- Use a Zener diode with $V_{br} = 5 \ldots 6\,V$ (5.6V)
  - Both Avalanche and Zener breakdown occur
  - Temperature behavior reduced

- Zener diode with avalanche in series with a forward biased junction

  ![Zener diode diagram](image1)

  t.c. about $-2\,mV/K$

  t.c. about $+2\,mV/K$

  Requires 6..7V

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**Buried Zener diode**

![Buried Zener diode diagram](image2)

- No degradation due to surface effects
  - less 1/f - noise
  - less sensitive to stress
**Forward biased junction**

\[
I_C = I_S \exp\left(qV_{BE} / kT \right)
\]

\[
qA_n^2 \bar{D}_n \quad N_B
\]

\[
CT^3 \exp\left[ -E_G(T) / kT \right] \quad kT / q \quad BT^\eta
\]

\[
I_{C0}(T / T_0)^\theta = C^\prime(T / T_0)^^\eta \exp\left[ qV_{BE} - E_G(T) \right] / kT
\]

\[
V_{BE}(T) = \frac{E_G(T)}{q} - \left[ \frac{E_G(T_0)}{q} - V_{BE}(T_0) \right] \frac{T}{T_0} + (\theta - \eta) \frac{kT}{q} \ln \left( \frac{T}{T_0} \right)
\]

**First-order approximation around T_0**

\[
V_{BE}(T) = \frac{E_G(T)}{q} - \left[ \frac{E_G(T_0)}{q} - V_{BE}(T_0) \right] \frac{T}{T_0} + (\theta - \eta) \frac{kT}{q} \ln \left( \frac{T}{T_0} \right)
\]

\[
V_{BE}(T) = \frac{E_G(T)}{q} - \left[ \frac{E_G(T_0)}{q} - V_{BE}(T_0) \right] \frac{T}{T_0} + (\theta - \eta) \frac{kT}{q} \ln \left( \frac{T}{T_0} \right)
\]

Taylor

\[
V_{GEff} = V_{G(0)} + (\eta - \theta)kT_0 / q
\]

- \( V_{BE} \) has negative t.c.
- \( V_{BE} \downarrow \) [t.c.] \( \uparrow \)
- \( V_{GEff} \) independent of \( V_{BE} \)
**Example**

Assume a transistor is biased at a constant current of 1 μA. For the transistor the following parameters apply: $I_S = 18 \, \text{mA}$, $XTI = 3$ and $V_{G0(0)} = 1.2\, \text{V}$.

What is the first-order temperature coefficient at $T_0 = 300\, \text{K}$?

$$V_{BE(300K)} = 640 \, \text{mV}$$
$$V_{Geff} = 1.2\, \text{V} + (3-0) \cdot 25.8\, \text{mV} = 1.28\, \text{V}$$

$$V_{Geff} = V_{G0(0)} + (\eta - 0)kT/q$$

$t.c. = -2.1 \, \text{mV/K}$

(Biasing a BE-junction)

- Bias current far below high-level injection ($I_C << I_{KF}$)
- Bulk resistances (made) negligible

$$I_C = I_S \left[ \exp\left(\frac{V_{BE}}{V_T}\right) - 1 \right] \left[ 1 - \frac{V_{BC}}{V_{AF}} - \frac{V_{BE}}{V_{AR}} \right]$$

- Nullor makes $V_{BC}=0$
- Nullor supplies $I_b$ and $I_{load}$
- Low beta no problem
- $V_{BE}$ is buffered
- $VAR$ remains

**Diagram**

Reference Sources: A. van Staveren and W.A. Serdijn
**Noise of a BE junction**

- $S_y$, noise-power density spectrum [V$^2$/Hz]
  \[ S_y = 4kT \left( \frac{1}{r_b} + \frac{1}{2g_m} \right) \]
- Collector shot noise and thermal noise of the base resistance dominate

- Assume $r_b=150$, $I_C=100\ \mu A$ and $V_{BE}=600\ mV$
  \[ 1 \frac{1}{2g_m} = 130 \]
  \[ S_y = 4kT \cdot 280\ \Omega \]

**Comparison**

- $R = \frac{600\ mV}{100\ \mu A} = 6000\ \Omega$

- Noise of a BE-junction is **20** times lower
- Output impedance is **25** times lower
**Proportional To Absolute Temperature**

- Difference of two junction voltages

\[ V_{\text{ref}} = V_{\text{BE1}} - V_{\text{BE2}} = \frac{kT}{q} \ln(n \cdot m) \]

**Example:**
\[
\text{n}=10 \rightarrow V_{\text{ref}} = \frac{kT}{q} \ln(10) \\
\text{m}=1 = T \cdot 198 \, \mu\text{V/K} \\
= 59.58 \, \text{mV} @ 300\,\text{K}
\]

Use as temperature sensor

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**Combination of a \( V_{\text{BE}} \) and \( V_{\text{PTAT}} \)**

\( V_{\text{BE}} \) has a negative t.c.
\( V_{\text{PTAT}} \) has a positive t.c.

Sum can have zero t.c.

**The Bandgap Reference**
The bandgap reference

Relates output voltage to the bandgap voltage at 0K

\[ V_{\text{ref}} = x \cdot \frac{E_G(0)}{q} \]

- Describe base-emitter voltage as:

\[ V_{BE}(T) = V_{\text{Geff}} - \left[ V_{\text{Geff}} - V_{BE}(T_0) \right] \frac{T}{T_0} \]

Use linear combination of base-emitter voltages

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Linear combination of $V_{BE}$

\[
a_1 V_{BE1} = a_1 V_{Geff} - a_1 \left[ V_{Geff} - V_{BE1}(T_0) \right] T / T_0 \\
a_2 V_{BE2} = a_2 V_{Geff} - a_2 \left[ V_{Geff} - V_{BE2}(T_0) \right] T / T_0 + \\
= (a_1 + a_2) V_{Geff} + 0 \cdot T / T_0
\]

$V_{ref}$

\[ V_{BE1} \]

\[ V_{BE2} \]

\[ V_{Geff} \]

\[ a_1 \]

\[ a_2 \]

$T$

NB: $a_2 < 0$

Bandgap Reference Example

\[ V_{REF} = a_1 V_{BE1} + a_2 V_{BE2} \]

\[ a_1 = 1 + \frac{R_2}{R_1} \]

\[ a_2 = -\frac{R_2}{R_1} \]

\[ a_1 + a_2 = 1 \]

But also: $V_{R1} = V_{BE2} - V_{BE1} = V_{PTAT}$

\[ V_{REF} = V_{BE2} + A_U V_{PTAT} \]
**Accuracy of $V_{ref}$**

$a_1, a_2$ : rely on matching

$V_{BE1}, V_{BE2}$ : several parameters are important

- $I_{S1}, I_{S2}$ : matching and absolute accuracy
- $I_{C1}, I_{C2}$ : use accurate bias techniques
- $\theta_1, \theta_2$
- $E_G, \eta, V_{AR}$ : given by process, good characterization required

*Key parameters* of device : $E_G, V_{AR}, I_S, \eta$

For accurate design these should be well-known!

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**Noise performance of Bandgap Reference**

- Noise of the bandgap reference is a weighted sum of the noise contributions of the $V_{BE}$

$S_{ref}$ is inversely proportional to the current consumption
**Power-Supply Rejection Ratio**

\[ PSRR = 20 \cdot 10^{\log \left( \frac{V_{r}}{V_{AF}} \frac{V_{ref}}{V_{s}} \right)} \]

unit: dB

**Design example 1V, 100 μA, BGR**

(Second-order compensated)

- Describe \( V_{BE_s} \) with a second-order polynomial

\[ V_{BE(T)} = V_{BE(T_0)} + x_1 (T-T_0) + x_2 (T-T_0)^2 \]

- Second (higher) order terms can only be changed by \( \theta \)

- Again use linear combination
- Two \( V_{BE_s} \) for second-order compensation
  - Different \( V_{BE_s} \) (1 order)
  - Different \( \theta \)'s (1 order)
**Block Schematic**

![Block Schematic Diagram]

Different $V_{BE}$s (1 order)
Different $\theta$’s (1 order)

$V_{ref} = 200$ mV

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**First implementation step**

![First Implementation Diagram]

Both $V_{BE}$s have negative t.c. ➔ scale factors must have opposite sign

- $a_1$ positive
- $a_2$ negative

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Implementation of VBE generators

At low temperatures $Q_a$ saturates $I_B$ of $Q_a$ degrades $I_{ref}$
Use cascade of NPNs

Implementation of the adder

- $V_{off}$ in series with $V_{ref}$
- Use differential input stage
- Use sized-emitter transistors

$V_{off}$ in series with $V_{ref}$
Low voltage level at input
Use differential input stage
Use sized-emitter transistors
Total Circuit

Where are the different blocks?

Measurement results

- $V_{\text{out}} = 194 \text{ mV}$
- Mean error = 1.5 ppm/K
- Output imp. = 43 $\Omega$
- Noise $< 80 \text{nV/\sqrt{Hz}}$
- $I_{\text{power}} = 100 \mu\text{A}$